Optimum Design of Nonlinear FET Amplifiers

CHAOYING GUO, MARC CAMIADE, DANIELLE ROUSSET, ANNIE CESSEY, JUAN JESUS OBREGON, AND ALAIN BERT

Abstract—**In this paper, an efficient approach to the optimum design of power amplifier stages is described. The impedances presented to the FET are optimized independently of the topology chosen for their realization. They are then synthesized by the usual methods of linear circuits. The proposed method has been applied to the design of broad-band power FET amplifiers. The realizations have given a good correlation between the theoretical and experimental results. Moreover, the method is being used in the optimum design of power FET multipliers.**

I. Introduction

OPTIMIZATION of nonlinear circuits will be a formidable task for microwave engineering in the coming years. A nonlinear circuit may be defined by at least one semiconductor device and a linear embedding circuit. Optimization of these circuits is usually done [1] by first fixing *a priori* a topology, and then optimizing the values of the linear elements afterwards. But is the topology chosen the best one? In fact, this design method of nonlinear circuits is directly derived from the linear method.

In this paper, a new approach to the optimization of nonlinear circuits is proposed. It allows a determination of the upper limits that can be achieved by a given active device. It has been successfully tested on power FET amplifier design. The proposed method is explained in Section II. In Section III the nonlinear FET model used is described along with the experimental setup developed to measure nonlinear characteristics of an FET with pulsed voltages; the results of the optimization are presented in Section IV. Finally, in Section V, the practical realization and experimental results are shown and compared with the theoretical predictions.

II. Proposed Optimization Method

Given a field-effect transistor (FET) defined by a time-dependent nonlinear model, let us suppose that we want to optimize the added power of the device, to use it in a stage power amplifier.

Manuscript received March 31, 1987; revised August 5, 1987. This work was supported in part by the Direction des Recherches et Etudes Techniques, France

C. Guo, D. Rousset, and J. Obregon are with IRCOM Université de Limoges - CNRS 87060, Limoges Cedex, France.

M. Camiade, A. Cessey, and A. Bert are with Thomson Hybrides et Microondes/DMH, 91300 Massy, France

IEEE Log Number 8717240.

In mathematical form, the device model describes the functional relationships between dependent and independent port variables. For an FET, these relations may be written in a general form valid for all nonlinear two-port circuits as

$$i_1(t) = F_{\mathrm{NL}}\left(v_1(t), v_2(t)\right)$$
$$i_2(t) = G_{\mathrm{NL}}\left(v_1(t), v_2(t)\right).$$

However, it is well known that the dependent variables in an FET are in fact functions of $v_{gs}(t)$ and $v_{ds}(t)$ (see Fig. 1). These latter voltages are now the independent variables, and we may write

$$i_1(t) = F_{\mathrm{NL}}\left(v_{gs}(t), v_{ds}(t)\right)$$
$$i_2(t) = G_{\mathrm{NL}}\left(v_{gs}(t), v_{ds}(t)\right). \tag{1}$$

From these equations it is clear that the behavior of the device is completely defined by a knowledge of the independent variables $v_{gs}(t), v_{ds}(t)$. In our example, let us suppose that the working frequency is ω_0.

Voltages at the gate and drain of an FET may be written in Fourier series:

$$v_{gs}(t) = v_{gs0} + V_{gs1}\cos\left(\omega_0 t + \psi_1\right) + v_{gs2}\cos\left(2\omega_0 t + \psi_2\right) + \cdots$$
$$v_{ds}(t) = v_{ds0} + v_{ds1}\cos\omega_0 t + v_{ds2}\cos\left(2\omega_0 t + \phi_2\right) + \cdots. \tag{2}$$

The transistor state is then defined by the vectors

$$\vec{v}_{gs} = \begin{bmatrix} v_{gs0} \\ v_{gs}e^{j\psi_1} \\ v_{gs}e^{j\psi_2} \end{bmatrix} \quad \text{and} \quad \vec{v}_{ds} = \begin{bmatrix} v_{ds0} \\ v_{ds1} \\ v_{ds}e^{j\phi_2} \end{bmatrix}.$$

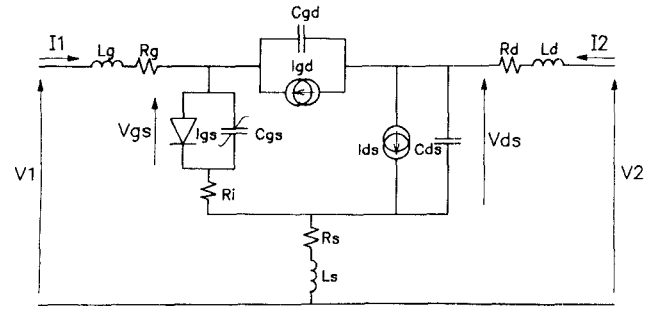
The vectors are the unknowns of the problem.

Introducing equations (2) in (1), the dependent variables (port currents) may be written in Fourier series as

$$\vec{I}_1 = \begin{bmatrix} I_{10} \\ I_{11}e^{j\gamma_1} \\ I_{12}e^{j\gamma_2} \end{bmatrix} \quad \text{and} \quad \vec{I}_2 = \begin{bmatrix} I_{20} \\ I_{21}e^{j\theta_1} \\ I_{22}e^{j\theta_2} \end{bmatrix}.$$

Defining now the maximum added power of the FET as the desired feature, one may write the function to be

0018-9480/87/1200-1348$01.00



Rg = 1.22ohm Rd = 0.6ohm Rs = 0.6ohm

Lg = 0.153nH Ld = 0.197nH Ls = 0.0329nH

Ri = 2.5ohm τ = 6.0pS

Cds = 0.123pF Cgd = 0.0433pF

Ids: Idss = 164.2mA m = −0.831 a = 0.124 b = 0.02316 p = 0.2182
Vpo = 2.038 Vdsp = 0.3951 w = 0 7367 Vphi = 0 853

Igd Ia = 322.657nA a = −0.7642 b = 0.0619 c = 5.0131 d = 0.8181
e = 1 3657

Ig: Is = 1.0nA α = 30.0

Cgs Cgso = 0 9437pF V_ϕ = 0 8V

Fig. 1. Nonlinear FET model

optimized as

$$P_{\text{add}} = P\left(\vec{V}_{gs}, \vec{V}_{ds}\right) = \frac{1}{2} R_e\left(-\vec{V}_{21}\cdot\vec{I}^*_{21} - \vec{V}_{11}\cdot\vec{I}^*_{11}\right).$$

A standard optimization routine [2] may be used to maximize P_{add} as a function of $\vec{V}_{gs}$ and $\vec{V}_{ds}$.

During the optimization iterative process, the variables are subject to two constraints: On the one hand, they must verify the nonlinear equations (1); on the other, their variations are limited by conditions allowing their physical realizability. Once optimization is achieved, bias voltages and FET loads are known from $\vec{V}_{gs}|_{\text{opt}}$ and $\vec{V}_{ds}|_{\text{opt}}$ as

bias voltages:

$$V_{gs0}|_{\text{opt}} \qquad V_{ds0}|_{\text{opt}}$$

FET loads:

at ω_0

$$\vec{Z}_g = \left(\frac{\vec{V}_{11}}{\vec{I}_{11}}\right)\Bigg|^*_{\text{opt}} \qquad Z_{21} = -\frac{\vec{V}_{21}}{\vec{I}_{21}}\Bigg|_{\text{opt}}$$

at $2\omega_0$

$$\vec{Z}_{12} = -\frac{\vec{V}_{12}}{\vec{I}_{12}}\Bigg|_{\text{opt}} \qquad Z_{22} = -\frac{\vec{V}_{22}}{\vec{I}_{22}}\Bigg|_{\text{opt}}.$$

Synthesis of the linear embedding circuit supporting these optimized variables may be now undertaken.

Our proposed process leads to global optimization of the overall nonlinear circuit. Indeed:

- The values of the access variables of the semiconductor device have been optimized for the desired objective function.
- The linear embedding network is synthesized to support these optimized variables as input signals at their own ports.

III. Nonlinear FET Model—Determination of the Nonlinearities

A. Large Signal Dynamic GaAs MESFET Model

The transistor used is a 0.5×800 μm FET. Fig. 1 shows the equivalent circuit model, in which four main nonlinear elements of GaAs MESFET have been considered. They are

- the input Schottky diode C_{gs} representing gate current in the gate–source junction;
- the gate–source capacitance C_{gs};
- the drain current source I_{ds};
- the drain–gate voltage-controlled current source I_{gd} describing the drain–gate avalanche current.

The current of the input Schottky diode is given by

$$I_g = I_s\left[\exp\left(\alpha_s V_{gs}\right) - 1\right]. \tag{3}$$

The drain current I_{ds} proposed by Tajima [3] has been modified as follows:

$$\begin{aligned}
I_{ds} &= f\left(V_{gs}, V_{ds}\right) = I_{dss}\cdot F_G \cdot F_D \\
F_G &= \frac{1}{K}\left[V_{gsn} - \frac{1-\exp\left(-mV_{gsn}\right)}{m}\right] \\
F_D &= 1-\exp\left[-\left(V_{dsn} + aV_{dsn}^2 + bV_{dsn}^3\right)\right] \\
V_{gsn} &= 1 + \frac{V'_{gs} - V_\phi}{V_p} \\
V_{dsn} &= \frac{V_{ds}}{V_{dsp}\left(1 + \dfrac{wV'_{gs}}{V_p}\right)} \\
V_p &= V_{\text{po}} + pV_{ds} + V_\phi \\
K &= 1 - \frac{1-\exp\left(-m\right)}{m} \\
V'_{gs} &= V_{gs}\left(t-\tau\right)
\end{aligned} \tag{4}$$

where I_{dss}, m, a, b, w, V_{dsp}, p, and V_ϕ are model parameters. V_{po} represents the pinchoff voltage and τ, the transit time under gate. The parameter V_ϕ has been put into the original relation to make the simulation better fit the measured curves in the saturation region, especially for V_{gs} around zero voltage, and G_{d0} has been neglected for the same reason.

The avalanche current I_{gd} is simulated by the following equation:

$$I_{gd} = I_{a0}\left(a + bV_{ds}^c\right)^{\left(c - dV_{gs}\right)} \tag{5}$$

where I_{a0}, a, b, c, d, and e are model parameters. It must be noted that the capacitances C_{gs} and C_{gd} may be modeled as functions of V_{gs} and V_{ds} from the total charge under the gate: Q_T. However, to a first approximation, C_{gd}

may be considered a constant, and C_{gs} may be represented by the well-known Schottky abrupt junction expression:

$$C_{gs} = \frac{C_{gs0}}{\sqrt{1 - \frac{V_{gs}}{V_{bi}}}}, \quad \text{for} \quad V_{gs} < V_{bi} \tag{6}$$

and for $V_{gs} \geq 0.8V_{bi}$,

$$C_{gs} = C_{gs}|_{V_{gs} = 0.8V_{bi}} = \text{const.}$$

B. Determination of the FET Model Elements

1) Determination of Linear Elements: In order to obtain more precise values, the measurements were performed in two steps. DC measurements are used to calculate the values of the resistances R_g, R_s, and R_d, while C_{gs0} of the gate junction and the values of other linear elements are determined from S parameter measurements in the 2–18-GHz range.

2) Determination of Nonlinear Current Sources: To minimize thermal and trapping effects, the pulsed setup shown in Fig. 2 has been developed.

Absorbers were needed to stabilize the FET from very low frequencies up to microwaves. Synchronous, short-pulse voltages V_1 and V_2 superimposed on the dc voltages V_{10} and V_{20}, which are around the operating point, are applied to the gate G and the drain D, respectively. These pulses have variable amplitudes, widths, and repetition rates.

In fact, the best method for characterizing a transistor in the whole plane $I_d = f(V_{gs}, V_{ds})$, is to bias the transistor at $V_{gs0} = 0$ V and $V_{ds0} = 0$ V and measure it by pulsed voltages for different temperatures.

A comparison between several repetition rates and widths shows that a 200-ns pulse width and a repetition rate of 10–100 kHz are best for minimizing the thermal and trapping effects. However these values depend on the FET used.

The drain currents I_{ds} measured by pulsed voltages and by dc voltages are both represented in Fig. 4. This setup makes it possible to measure independently the different current sources as functions of the external applied voltages:

$I_{ds}(V_1, V_2)$: field-effect current

$I_g(V_1)$: Schottky current

$I_{gd}(V_1, V_2)$: avalanche current.

These currents, which are functions of V_1 and V_2, are then transformed to internal current sources depending on V_{gs} and V_{ds}, by taking into account the voltage drops in R_g, R_s, and R_d. One obtains

$$I_{ds} = f(V_{gs}, V_{ds})$$

$$I_g = g(V_{gs})$$

$$I_{gd} = h(V_{gs}, V_{ds}).$$

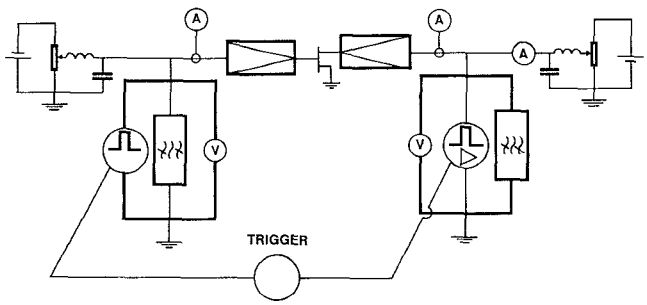
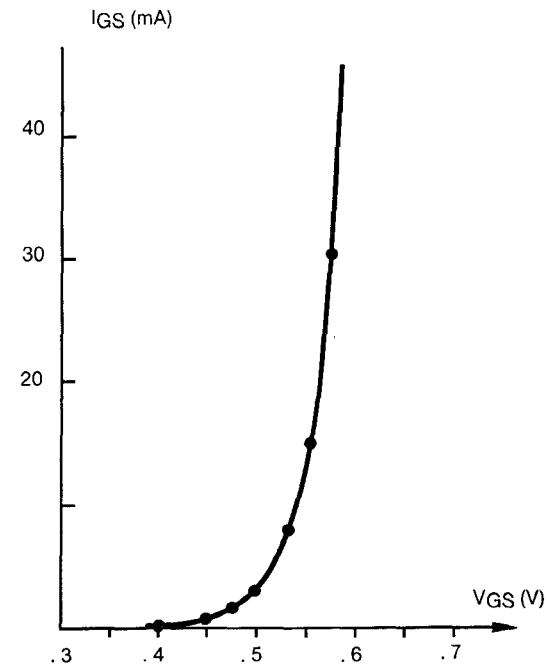
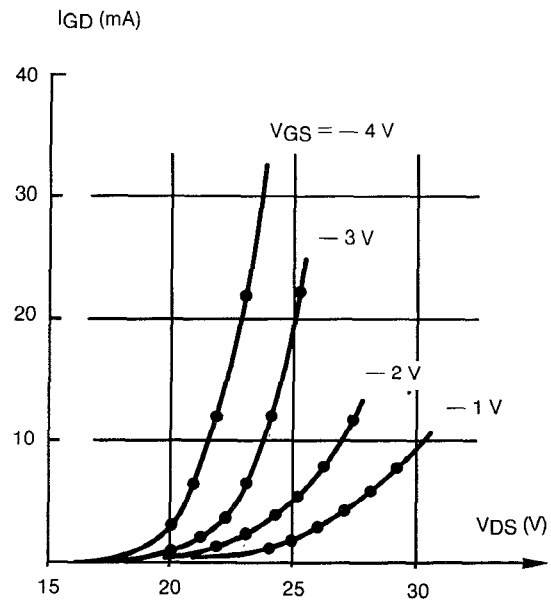


Fig. 2. Pulsed measurement setup.



(a)



(b)

Fig. 3. (a) Gate current I_g as a function of gate voltage V_{gs}. (b) Avalanche current I_{gd} as a function of gate and drain voltages V_{gs} and V_{ds}. • Measured. ——— Fitted.

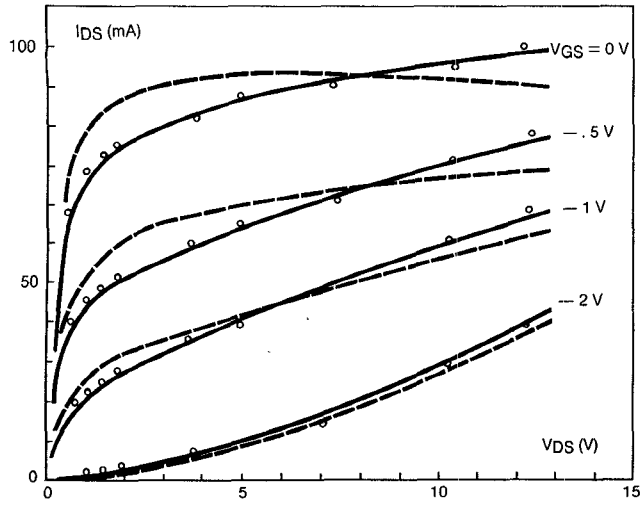


Fig. 4. Drain current I_d, measured by pulse voltages with 200-ns widths and 100-kHz repetition rates. ———— Pulsed. O Measured. ---- dc.

These experimental curves are now fitted to the previously given expression.

Experimental points are plotted in Figs. 3 and 4 together with the simulated curves based on the (3), (4), and (5) for comparison.

IV. Optimization of the Amplifier Stage

The objective is to design a power amplifier giving the maximum added power covering X- and K_u-band. Since the bias voltages must be kept constant, they are optimized at 18 GHz and taken as constant at the other frequencies.

Optimization of the Amplifier

Let $\vec{V}_{1i}$, $\vec{V}_{2i}$, $\vec{I}_{1i}$, and $\vec{I}_{2i}$ be the complex voltages and currents at frequencies if_0 $(i=1,2,3,\cdots)$ and ports 1,2. The problem is to maximize

$$P_{\text{added}} = \frac{1}{2}\,\text{Re}\left(-\vec{V}_{21}\cdot\vec{I}_{21}^{*} - \vec{V}_{11}\cdot\vec{I}_{11}^{*}\right)$$

under the following constraints [4]:

$$\text{Re}\left(\frac{\vec{V}_{1i}}{\vec{I}_{1i}}\right)\begin{cases} > C_i, & i=1 \\ \leqslant C_i, & i=2,3,\cdots \end{cases} \quad \text{at port 1}$$

$$\text{Re}\left(\frac{\vec{V}_{2i}}{\vec{I}_{2i}}\right) \leqslant D_i, \qquad i=1,2,3,\cdots \quad \text{at port 2}$$

where C_i, D_i $(i=1,2,3,\cdots)$ are constants $(C_i \geqslant 0,\ D_i \geqslant 0)$.

In the first procedure of optimization, C_i and D_i $(i=1,2,3,\cdots)$ can be chosen equal to zero. If the optimum impedances at ports 1 and 2 are difficult to realize, C_i and D_i must be changed to the positive constants.

Optimum design is achieved by an iterative procedure. A quasi-Newton method called the variable metric method (Broyden–Fletcher–Goldfarb–Shanno [BFGS] method) is used as an optimization method for minimizing the objective function $F(X)$, where $X^T=(x_1,x_2,\cdots,x_n)$. The vector X represents the set of unknowns. The method is logically divided into two parts. The first part has the task of selecting a direction d

$$d_k = -H_k \nabla F(X^k) \tag{7}$$

where

$$H_{k+1} = H_k + \left[1+\frac{\gamma_k H_k \gamma_k}{\delta_k^T \gamma_k}\right]\frac{\delta_k \delta_k^T}{\delta_k^T \gamma_k} - \frac{\delta_k \gamma_k^T H_k + H_k \gamma_k \delta_k^T}{\delta_k^T \gamma_k}$$

$$\delta_k = X^{k+1} - X^k$$

$$\gamma_k = \nabla F(X^{k+1}) - \nabla F(X^k)$$

k: number of iterations

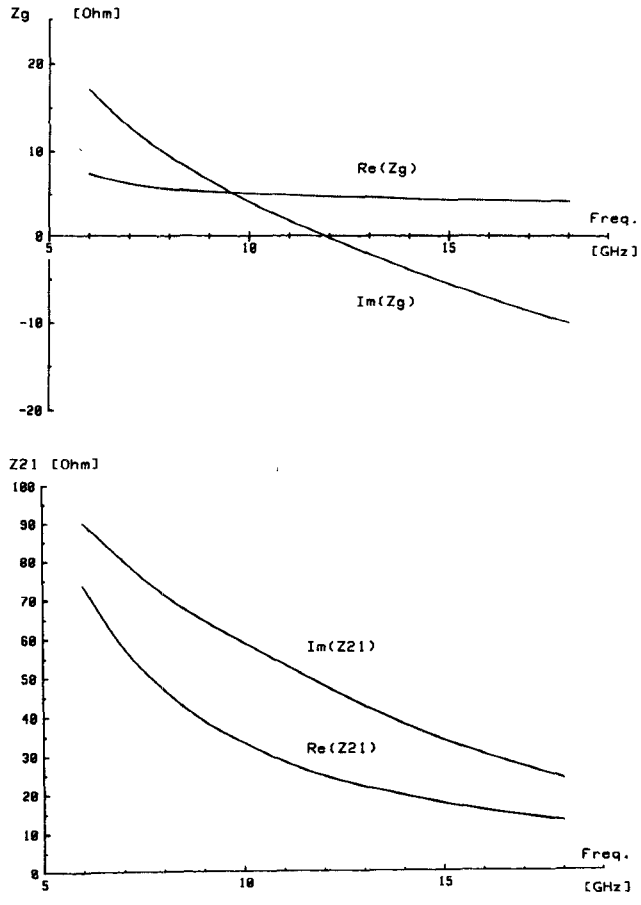


Fig. 5. Theoretical impedances at fundamental frequency ω_0.

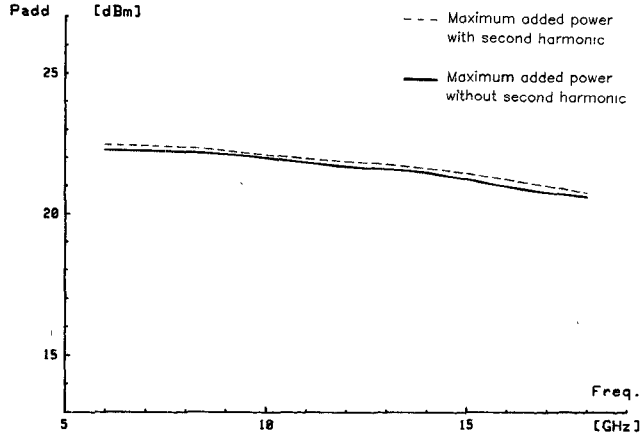


Fig. 6. The influence of second harmonic frequency for the result of optimization.

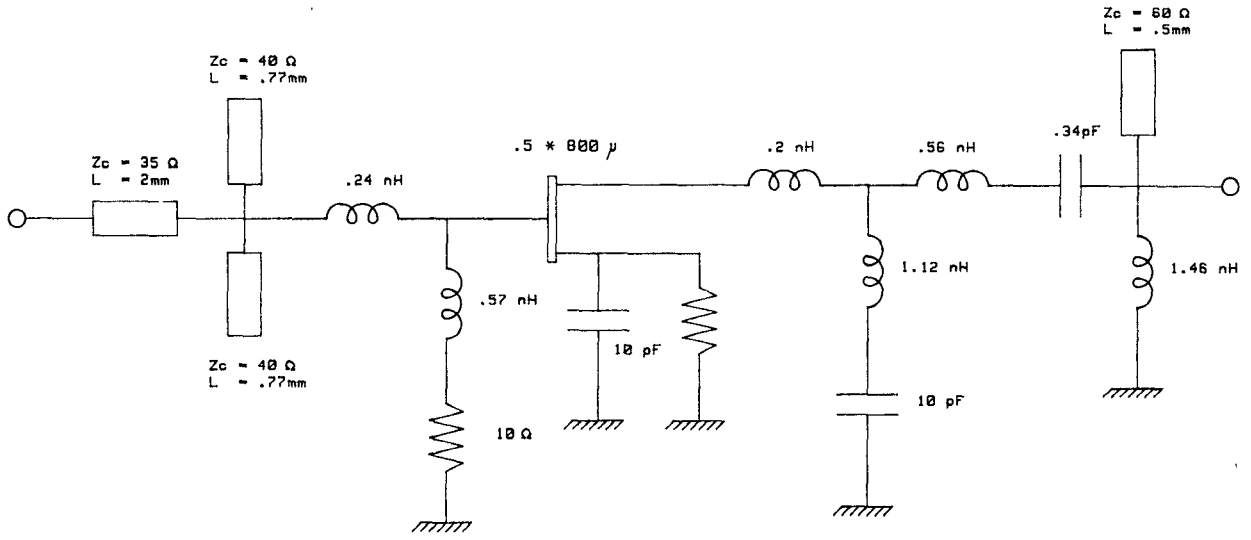


Fig. 7 Equivalent circuit of one-stage power amplifier

while the second part searches along the direction d_k to find the minimum of the function $F(X)$ along d_k. The convergence speed of this method is faster than other published methods when the number of unknowns is greater than 10.

From (7), the derivatives of the objective function $\nabla F(X)$ have to be calculated for determining the searching direction d. We can use numerical differentiations in place of derivatives, but the long CPU time and poor accuracy cannot be avoided.

In fact, from (1),

$$i_1(t) = F_{\mathrm{NL}}\left(v_{gs}(t), v_{ds}(t)\right)$$

$$i_2(t) = G_{\mathrm{NL}}\left(v_{gs}(t), v_{ds}(t)\right)$$

and the equations of nonlinear elements (3), (4), (5), and (6), all derivatives of the objective function, could be presented in analytical form. So the problems of long computing time and accuracy are solved.

In order to make the unknowns have the same dimensions, $\mathrm{Re}(\vec{V}_{gsj})$, $\mathrm{Im}(\vec{V}_{gsj})$, $\mathrm{Re}(\vec{V}_{dsj})$, and $\mathrm{Im}(\vec{V}_{dsj})$ $(j = 0,1,2,\cdots,N)$ are chosen as the variables. In the procedure of optimization, we first select initial values $\mathrm{Re}(\vec{V}_{gsj})$, $\mathrm{Im}(\vec{V}_{gsj})$, $\mathrm{Re}(\vec{V}_{dsj})$, $\mathrm{Im}(\vec{V}_{dsj})$, V_{gs0}, and V_{ds0} and then use circuit analysis to find $\vec{I}_{1i}$ and $\vec{I}_{2i}$, $i = 1,2,3,\cdots$. Other feasible points are then calculated by using the optimization algorithm.

Optimized bias voltages V_{gs0}, V_{ds0} and optimum impedances Z_{ki} are finally obtained for $k = 1,2$; $i = 1,2,3,\cdots$. In our design, we have obtained

$$V_{gs0} = -1\,\mathrm{V}$$

$$V_{ds0} = 10\,\mathrm{V}$$

at 18 GHz, and they have been kept constant at other frequencies. Fig. 5 gives the theoretical impedances at fundamental frequency ω_0, $\vec{Z}_g$ and $\vec{Z}_{21}$. The influence of higher harmonics (second and so on) is very small since the maximum added power occurs in the "quasi-linear" region (around 1 dB gain compression). The effect of the second harmonic is shown in Fig. 6.

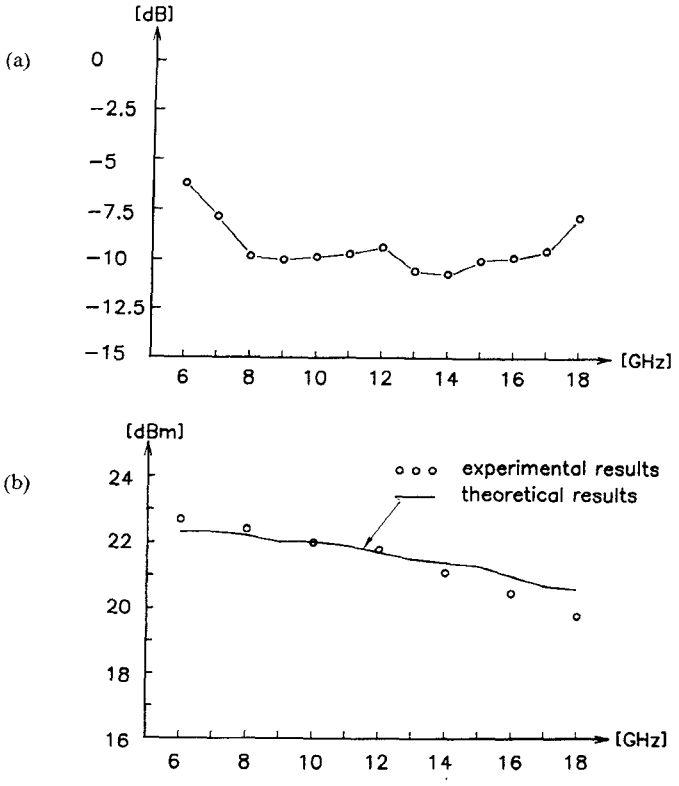


Fig. 8. (a) Output return loss of the one-stage power amplifier (b) Maximum added power of the one-stage power amplifier.

V. Amplifier Realization—Experimental Results

FET's from different sources have been characterized and optimized by using the previous analysis. Taking into account the results given by the nonlinear optimization, linear embedding circuits have been synthesized.

Fig. 7 shows the circuit of a one-stage medium power amplifier using a typical 0.5×800 μm FET. The output

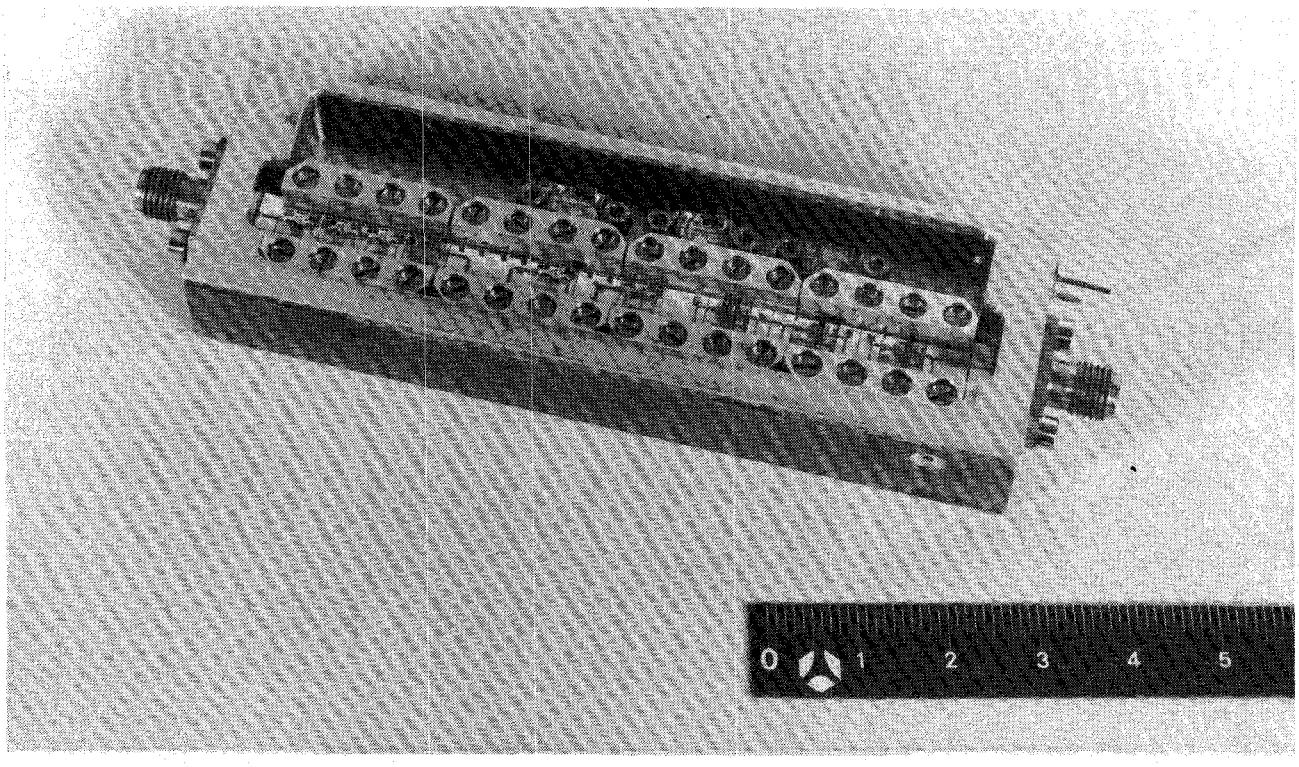


Fig. 9. 26-dBm amplifier.

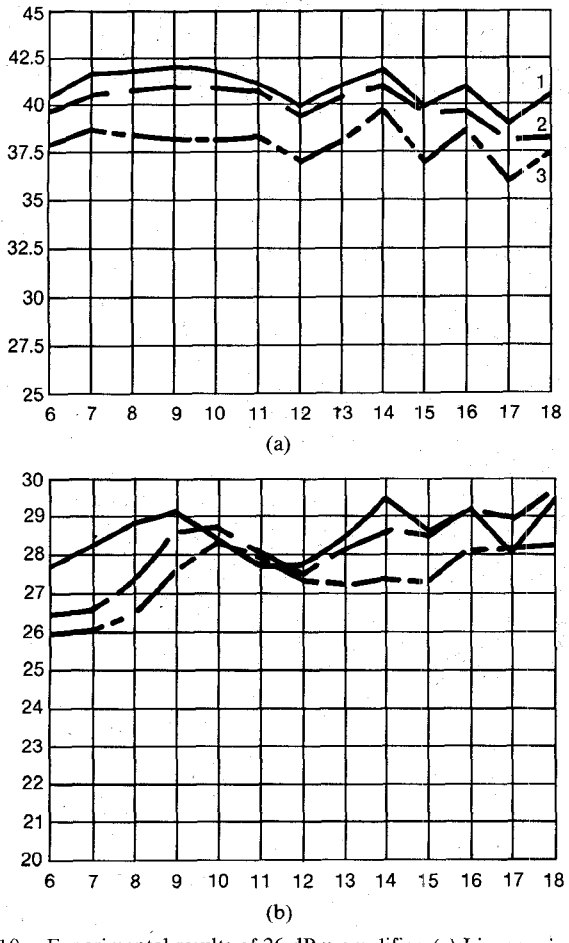


Fig. 10. Experimental results of 26-dBm amplifier. (a) Linear gain (dB). (b) Output power (dBm), with $P_{in} = -5$ dBm. Frequency is in GHz. The following temperatures were used: $1 = -40°$; $2 = 20°$; $3 = 90°$.

return loss is given in Fig. 8(a), and the computed curve and experimental points representing the maximum added power versus frequency are shown in Fig. 8(b). Since experimental results include the circuit losses, the correlation is better than 1 dB. The same procedure has been used to design the output stages of a 26-dBm amplifier (Fig. 9). Experimental results of this amplifier are given in Fig. 10.

VI. Conclusions

In this paper, a new approach to the optimization of nonlinear amplifiers has been described. The key point of this approach is that no topology of the embedding linear network is to be chosen *a priori*. Hence the performances of the active devices calculated by this method are the upper limits that can be achieved by the given active device. To validate the proposed method, it has been applied to the design of a broad-band amplifier. Practical results have shown very good correlation with the theoretical prediction.

The method is being extended to the optimum design of other components such as power multipliers and converters.

References

[1] V. Rizzoli, A. Lipparini, and E. Marazzi, "A general purpose program for nonlinear microwave circuit design," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-31, pp. 762–769, Sept. 1983.

[2] M. J. D. Powell, *Nonlinear Optimization*. New York: Academic Press, 1982.

[3] Y. Tajima and P. Miller, "Design of broad-band power GaAs FET amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-32, pp. 621–627, Mar. 1984.

[4] M. C. Albuquerque, C. Guo, and J. Obregon, "A new approach to fundamental frequency analysis and optimization of nonlinear microwave circuits," in *Proc. 15th E.M.C.*, Sept. 1985, pp. 515–520.

✠

Chaoying Guo was born in Beijing, China. She received the diploma in electrical engineering from Beijing Normal University in 1982. From 1982 to 1985, she worked on microwave low-noise GaAs FET amplifiers, oscillators stabilized by dielectric resonators, and computer-aided design of microwave circuits at Beijing Normal University.

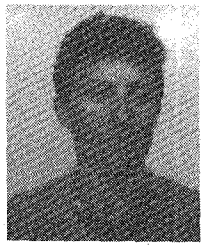
Since 1985, she has been with the Institut de Recherches en Communications Optiques et Microondes at the University of Limoges, France. Currently, she is working toward the Ph.D. degree in electrical engineering. Her main area of interest is the modeling of microwave GaAs FET's, nonlinear analysis, and optimization of microwave circuits.

✠

Marc Camiade was born in Mugron, France, in 1958. He received the Dipl. Ing. degree from the Institut National des Sciences Appliquées, Toulouse, France, and the "Diplome d'Etudes Approfondies" in microelectronics from the University Paul Sabatier, Toulouse, in 1981.

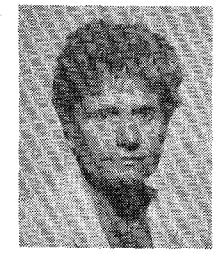
He joined the Thomson Microwave Micro electronic Division in 1982. His early work concerned dielectric resonator oscillators and voltage-controlled oscillators. He is currently working on low-noise and medium power amplifiers in hybrid as well as in monolithic form.

✠



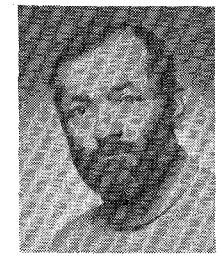
Danielle Rousset received the Ph.D. degree in electronics and communication from Limoges University in 1976. From 1974 to 1981, she was "Maitre Assistant" of electronics at the University of Algiers, Algeria.

Then, she joined Limoges University as "Maitre de Conférence" in the Institut de Recherches en Communications Optiques et Microondes (IRCOM). At this time, her main area of interest is the nonlinear modeling of microwave GaAs FET's.



Annie Cessey worked as a technician in the Thomson Tube Division on traveling wave tubes from 1959 to 1975. She then joined, as an engineer, the Microwave Microelectronic Division working on solid-state circuits. Her primary interest has been the study of traveling wave divider/combiner and phase shifters. She is now working on medium power amplifiers.

✠

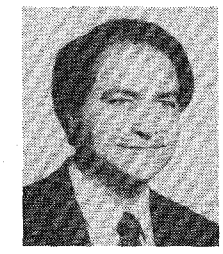


Juan Jesus Obregon was born in 1939. He worked as a technician in the radar division of Thomson-CSF in 1961. He received the E.E. degree from the Conservatoire National des Arts et Métiers, Paris in 1967.

He joined RTC Laboratories in 1969, where he worked on oscillator combiners. Then he joined the DMH division of Thomson-CSF and became Group Leader of the active circuits laboratory. He received the Ph.D degree from the Université de Limoges in 1980.

Since 1981, he has been Professor at the Université de Limoges, where he heads a research team involved in microwave active circuit theory and design. His field of interest is the nonlinear analysis, optimization, and design of microwave noisy and noiseless circuits.

✠



Alain Bert graduated from the Ecole Nationale Supérieure des Télécommunications in Paris and received the M.S. degree from Stanford University.

Then, he worked for the Thomson Tube Division on high-power klystron and traveling wave tubes. He joined the research lab, working on surface acoustic wave memory and power solid-state devices. He is now in charge of the hybrid and monolithic product development department in Thomson Microwave Microelectronic Division.